

## ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

**Title of  
Invention**

A METHOD, SYSTEM, AND COMPUTER PROGRAM  
PRODUCT FOR GENERATING AND VERIFYING ISOLATION  
LOGIC MODULES IN DESIGN OF INTEGRATED CIRCUITS

Application Number :

Confirmation Number:

First Named Applicant: Bhanu KAPOOR

Attorney Docket Number: Q82851

Art Unit:

Examiner:

Search string: ( 5483176 or 6083271 or 6600358 or 6711719 or 6717452 ).pn

### US Patent Documents

**Note: Applicant is not required to submit a paper copy of cited US Patent Documents**

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
	1	5483176	1996-01-09	Rodriguez			
	2	6083271	2000-07-04	Morgan			
	3	6600358	2003-07-29	Chan			
	4	6711719	2004-03-23	Cohn			
	5	6717452	2004-04-06	Carpenter			

### Signature

Examiner Name	Date